NEWSLETTER

(January 2020 - February 2021)

ISSUE #1

MORAL

Export free rad-hard microcontroller for space applications

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H2020 MORAL Project

DEAR READER,

Welcome to the first newsletter of the MORAL project.

MORAL project started in January 2020 with the aims to radically change the European space landscape by opening new business opportunities, offering products that are more affordable, more reliable, and provide more performance than traditional LEON or ARM approaches. In this sense, MORAL is focused on the development of a complete European, International Traffic in Arms Regulations (ITAR) free, high performance, 32-bit microcontroller for space applications, focused on small satellites, flight control, and payload computers. In MORAL the novel IHP Peaktop architecture extended to include a Floating-Point Unit (FPU) and provide support to Digital Signal Processing (DSP). Furthermore, novelties such as an unprecedented rad-hard 12-bit, 8-channel ADC and DAC converter, large rad-hard on-chip memory, SpaceWire, M1553, Pulse-Width Modulators (PWM), and other peripherals will be also planned to be included.

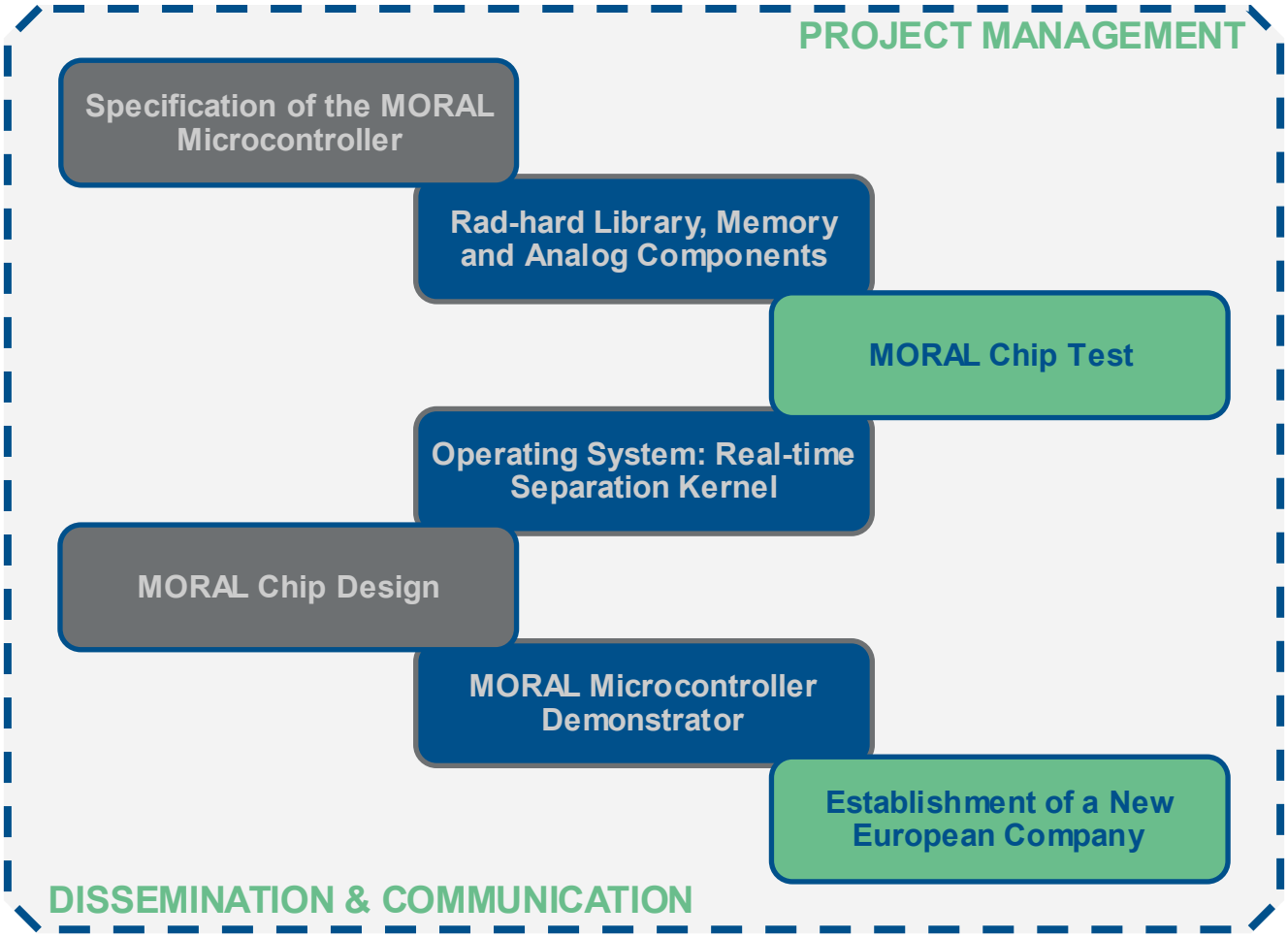
In this first issue of the MORAL newsletter we report the progress of the project gained in the first 14 months of work.

We hope you enjoy reading our newsletter and invite you to check our website (moral-project.eu) regularly and our social media, or contact us directly for more information.

Yours sincerely,

The MORAL team!

MORAL PROJECT IN A NUTSHELL



MORAL CONSORTIUM

Project Coordinator

IHP GMBH - Innovations for High Performance Microelectronics
LEIBNIZ - INSTITUT FUER INNOVATIVE MIKROELEKTRONIK
(Germany)

REDCAT DEVICES SRL
(Italy)

SYSGO GMBH
(Germany)

THALES ALENIA SPACE ESPANA, SA
(Spain)

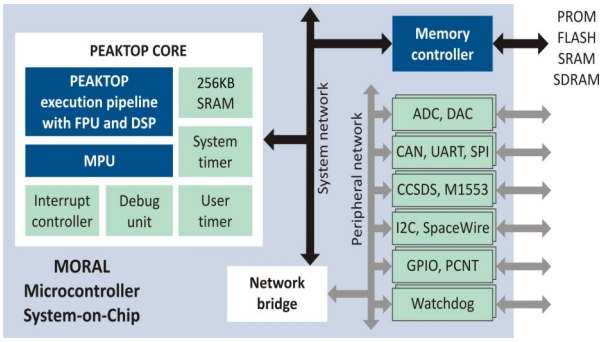
ABSINT ANGEWANDTE INFORMATIK GMBH
(Germany)

MORAL MAIN RESULTS ACHIEVED IN THE FIRST 14 MONTHS

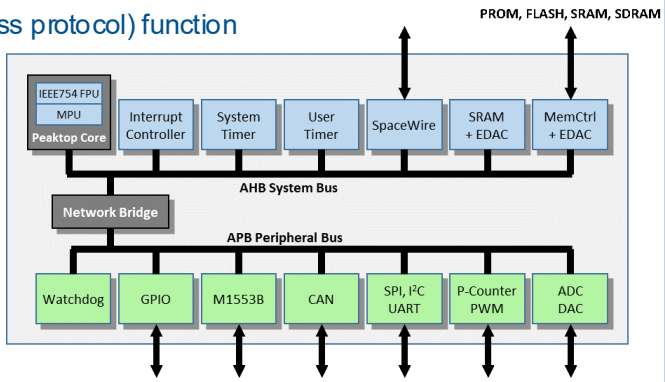
Specification of the MORAL Microcontroller

One of the major outcomes of the first 6 months of the project was the mircrocontroller specificaion. Here you can see a summary of the features.

- **Core**: 32-bit CPU with FPU compliant to IEEE 754-2008 standard, DSP support, and 2-level Memory Protection Unit. The new ISA is fully **orthonogonal**, instructions and addressing modes equally treat each GPR, **regular**, machine modes up to 128 bytes, and **circular,** last GPR is a "logical" neighbor to the first GPR.
- **Memory**
  - 32-bit on-chip SRAM
  - 256/512KB of on-chip SRAM extended with EDAC (error detection and detection)
  - Memory controller for accessing external memories (PROM, EEPROM, and SRAM)
- **Clock, reset, and supply**
  - 1.2V core supply and 3.3V analog components and I/O supply
  - 50MHz system clock
  - 200MHz peripherals clock for PWM and SpaceWire
  - 10 clock cycle power-up and reset procedures



- **Operating modes**
  - System mode: all instruction and registers available
  - User mode: system instructions and special registers not accessible
- **Debug mode**
  - Read/write access to GPRs, special registers, and all other peripherals' registers, as well as internal and external memory and I/O devices
  - Access over AHB master peripherals (UART or SpaceWire)
- **Communication interfaces**
  - 2x SpaceWire: include RMAP (remote memory access protocol) function
  - 4x UART interfaces
  - 2x SPI interfaces
  - 2x I^2C interfaces: 8-bit oriented up to 1Mbit/s bidirectional and up to 5Mbit/s unidirectional
  - 2x CAN 2.0B interfaces: up to 1 Mbit/s
  - 1 x MIL-STD 1553C bus interface: raw data rate of 1 Mbit/s



- **Analog components**
  - 2x 12-bit DAC converters
  - 1x 12-bit ADC converter: 8 single-ended or 4 differential channels
- **Other components**
  - 32-bit timers connected to AHB system bus: 2 system timers and 4 user timers
  - 1x interrupt controller (32 interrupt lines)
  - 4x pulse counters
  - 1x watchdog timer
  - 1x PWM generator: independent 8-channel or complementary in up to four 2-channel pairs
  - 64x GPIO ports (shared with internal peripherals I/Os)
- **Technology**: IHP SG13RH (S) process
- **Packaging**: 208 pin ceramic
- **Rad-Hard Spec**
  - Total ionizing dose (TID) 100 krad (Si)
  - Single event upset (SEU) for the processor's digital core >30 MeVcm²/mg
  - Single event latch-up (SEL) >60 MeVcm²/mg

MORAL MAIN RESULTS ACHIEVED IN THE FIRST 14 MONTHS

MORAL Developments Overview

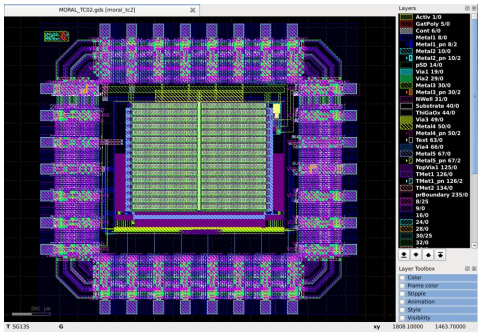
MORAL has achieved very good technical and non-technical progress in the first 12 months.

- The complete PEAKTOP ISA has been developed. The corresponding RTL model of the processor has been developed and verified in simulation.
- Performance and capabilities improvements of the base PEAKTOP has been carried out with the re-design of the MPU and the complete design of the IEEE 754 compliant FPU unit.
- The MIL-STD 1553 IP was developed and integrated with all other digital IPs.
- The MORAL processor and the new-generation IPs undergo exhaustive verification code.
- A co-verification, simulation, and testing platform are used in MORAL, allowing parallel hardware and software design and verification.
- Verification and integration tests are being executed at every step of the design, from RTL simulations to post-synthesis, and more recently with FPGA emulation of the MORAL core.
- The complete digital part of the microcontroller has been finalized and verified in simulation.
- The radiation-hard standard cell library is available.
- High-level methods are applied to provide additional protection (ECC for memory, HDL coding style for high reliability, TMR redundancy).
- The processor core has been initially synthesized using the radiation-hard library and back-annotated in simulation.
- The SRAM blocks were designed and simulated. The first MORAL test chip containing the SRAM blocks was produced and evaluated at the silicon level (on-wafer testing).
- A second MORAL test chip containing a preliminary 10-bit DAC has been taped-out and is ready for testing. The final 12-bit DAC design will be completed after completing the 10-bit DAC evaluation.
- The third test chip containing the ADC is under preparation and should be available in the following months.
- An initial Open Source software toolchain is available for download on the project website.
- The C compiler (CompCert) development for the PEAKTOP ISA is also in progress.
- The OS support for the processor PEAKTOP started in the last quarter of the year.
- On the non-technical side, many dissemination activities have been performed, and an exploitation plan draft has been generated.

AN INSIDE LOOK AT MORAL DEVELOPMENTS

Rad-hard Library, Memory, and Analog Components

The MORAL microcontroller is expected to run mainly on satellites housekeeping operations. The major part of foreseen orbits are LEOs and GEOs, thus limiting the expected TID up to 300 krad (Si) (less than 100 krad (Si) for VLEOs) and SEL to 60 MeV*cm2/mg (Si). The required robustness is achieved by using the IHP 130nm CMOS process and leveraging the RHBD approach. The full rad-hard standard cell library has been designed and provided for the digital ASIC flow.

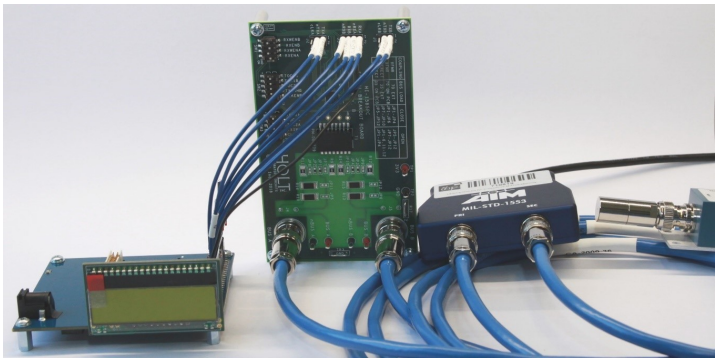


MORAL memory requirements demand an extremely reliable device from an SEU point of view. A specific memory architecture (1-bit-only) with a dedicated decoding scheme has been adopted to avoid any double error.

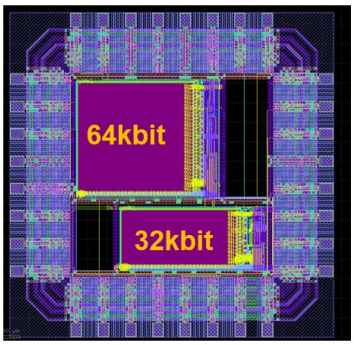
Due to the architectural novelties employed in the DAC design, a preliminary 10-bits version was designed to evaluate the resistive matrix behavior before the final 12-bit version development. The image on the right shows the 10-bit DAC layout.

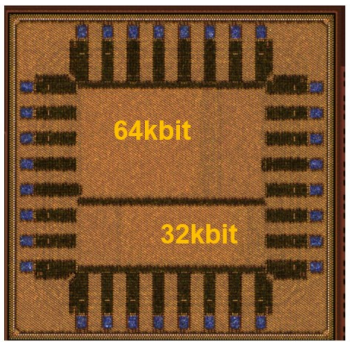
MORAL Chips Testing

Techniques for efficient verification, testing, and debugging of the MORAL chip are an important aspect of the project development. At this stage, functional RTL simulations are conducted to verify all the specific characteristics of the MORAL chip and the peripheral's intergradation. Additionally, to reduce MORAL's microcontroller development risk, an FPGA prototyping of the processor and its peripherals was developed for testing. On the right is the test setup for the MIL-STD 1553 IP. The FPGA prototype will be shared with partners to help develop the OS and the compiler.



The first test chip containing the single bit 64kbit and 32kbit SRAM blocks is ready for wafer testing. The images below show the SRAM test chip layout, the fabricated chip, and lab where the wafer tests are conducted.





High-level Language Compilers and Real Time Separation Kernel

The C compiler porting for the Peaktop architecture was carried out. For all chosen instruction selections schemes, a mathematical proof must be provided that guarantees the semantic preservation of CompCert for all transformations on or translations between intermediate representations. The resulting proof scripts are part of the CompCert source code. Moreover, the binary utilities were implemented by adapting and extending the publicly available GNU binutils for the new target platform. These adaptations will be published under the GNU GPL license and integrated into MORAL distribution.

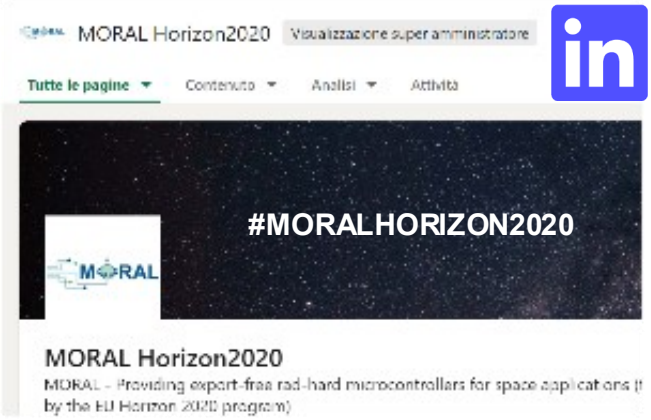
In the OS development, a RTSK (real time separation kernel) architecture is used. It allows the technical separation of the kernel, ASP (architecture support package), and PSP (platform support package) to design a novel RTSK for MPU based platforms. These separate components allow the kernel to be purely generic, hence portable. These developments are undergoing.

STAY TUNED WITH UPCOMING NEWS AND RESULTS...

THE MORAL OFFICIAL WEBSITE IS NOW ONLINE!

A VIRTUAL SPACE, RICH IN DATA, RESULTS AND NEWS ABOUT THE MORAL PROJECT AND NEWS FROM SPACE!

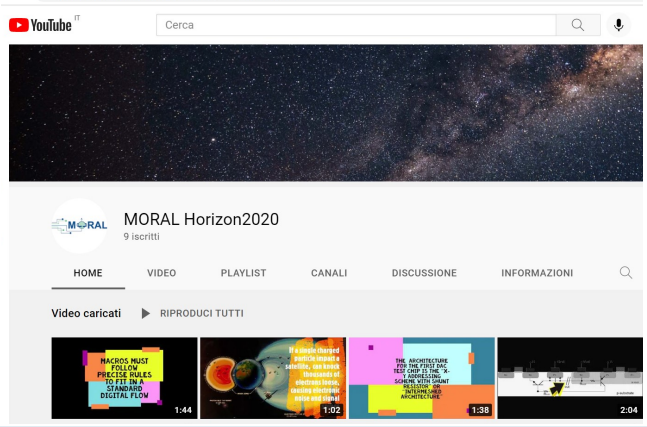
CLICK HERE TO STAY TUNED!



MORAL IS ON LINKEDIN!

THE MOST POWERFUL SOCIAL NETWORK IN THE BUSINESS SECTOR HAS BEEN SELECTED TO ACHIEVE MORAL EXPLOITATION SCOPES!

FOLLOW OUR POSTS TO GET INFORMED ABOUT ANY NEW COMMERCIAL POTENTIAL OFFERED BY MORAL!



A **MORAL YouTube Channel** HAS BEEN ACTIVATED IN ORDER TO SHARE WITH THE COMMUNITY SCIENTIFIC AND TECHNICAL VIDEOS ABOUT THE MORAL ACTIVITIES!

SUBSCRIBE THE MORAL YOUTUBE CHANNEL!

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MORAL

PROJECT CONTACTS

IHP GMBH - Innovations for High Performance Microelectronics LEIBNIZ - INSTITUT FUER INNOVATIVE MIKROELEKTRONIK (Germany)
Contact person: Kuentzer Felipe Augusto
E-mail: kuentzer@ihp-microelectronics.com

REDCAT DEVICES SRL (Italy)
Contact person: Cristiano Calligaro
E-mail: c.calligaro@redcatdevices.it

SYSGO GMBH (Germany)
Contact person: Axel Von Blomberg
E-mail: axel.von.blomberg@sysgo.com

THALES ALENIA SPACE ESPANA, SA (Spain)
Contact person: Manuel Sanchez
E-mail: manuel.sanchez@thalesaleniaspace.com

ABSINT ANGEWANDTE INFORMATIK GMBH (Germany)
Contact person: Michael Schmidt
E-mail: mschmidt@absint.com

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