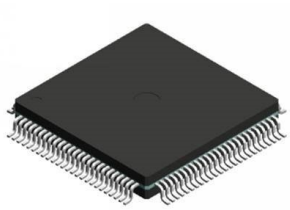
MORAL Peakrad SG13H (S)

MORAL Rad-Hard Peakrad 32-bit MPU+FPU, 256/512KB SRAM +EDAC, SpaceWire, MIL-STD 1553C, 12-bit ADC, 12-bit DAC, SPI, I^2C, CAN 2.0B

Datasheet - specification data

Features

- Core: **MORAL Peakrad 32-bit** CPU with FPU compliant to IEEE 754-2008 standard, DSP extension, and 2-level Memory Protection Unit. The new ISA is fully **orthogonal**, instructions and addressing modes equally treat each GPR, **regular**, machine modes up to 128 bytes, and **circular,** last GPR is a "logical" neighbor to the first GPR.
- Memory
  - 32-bit on-chip SRAM
  - 256/512KB of on-chip SRAM extended with EDAC (error detection and correction)
  - Memory controller for accessing external memories (PROM, EEPROM, and SRAM)
- Clock, reset, and supply
  - 1.2V core supply and 3.3V analog components and I/O supply
  - 50MHz system clock
  - 200MHz peripherals clock for PWM and SpaceWire
  - 10 clock cycle power-up and reset procedures
- Operating modes
  - System mode: all instruction and registers available
  - User mode: system instructions and special registers not accessible
- Debug mode
  - Read/write access to GPRs, special registers, and all other peripherals' registers, as well as internal and external memory and I/O devices
  - Access over AHB master peripherals (UART or SpaceWire)
- 32-bit timers connected to AHB system bus: 2 system timers and 4 user timers



208 pin ceramic package

*illustrative image

- Communication interfaces
  - 2x SpaceWire: include RMAP (remote memory access protocol) function
  - 4x UART interfaces
  - 2x SPI interfaces
  - 2x I^2C interfaces: 8-bit oriented up to 1Mbit/s bidirectional and up to 5Mbit/s unidirectional
  - 2x CAN 2.0B interfaces: up to 1 Mbit/s
  - 1 x MIL-STD 1553C bus interface: raw data rate of 1 Mbit/s
- 2x 12-bit DAC converters
- 1x 12-bit ADC converter: select from 8 single-ended or 4 differential channels
- 1x interrupt controller (32 interrupt lines)
- 4x pulse counters
- 1x watchdog timer
- 1x PWM generator: independent 8-channel or complementary in up to four 2-channel pairs
- 64x GPIO ports (shared with internal peripherals I/Os)
- Technology: IHP SG13RH (S) process
- Rad-Hard Spec
  - Total ionizing dose (TID) 100 krad (Si)
  - Single event upset (SEU) for the processor's digital core >30 MeVcm²/mg
  - Single event latch-up (SEL) >60 MeVcm²/mg