DEMONSTRATOR BOARD

A functional demonstrator board is planned (see Fig. 4), in order to show the operation of the MORAL chip in a real system.

This board will be used for dissemination activities, e.g., presentation on fairs.

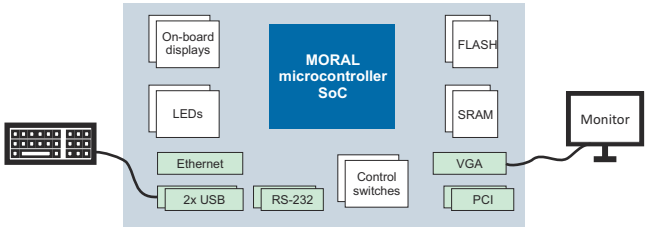

Fig. 4: MORAL functional demonstrator board

PROJECT PARTNERS

innovations for high performance microelectronics

EMBEDDING INNOVATIONS

RedCat Devices

AbsInt

ThalesAlenia Space
A Thales / Finmeccanica Company

MORAL

Export-restriction-free Rad-hard Microcontroller for Space Applications

PROJECT PARTNERS

1. IHP GmbH, Germany - Coordinator
2. REDCAT DEVICES SRL, Italy
3. SYSGO GmbH, Germany
4. THALES ALENIA SPACE ESPANA, SA, Spain
5. AbsInt Angewandte Informatik GmbH, Germany

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Disclaimer: this flyer reflects only the authors' views and excludes the EC and REA from responsibility.

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Duration: 40 months
Project number: 870365
Costs: EUR 2.999.881,25

Funded by the European Commission

European Commission

THE MORAL PROJECT

OBJECTIVES

Develop a completely European, ITAR-free, Rad-hard Microcontroller for Space Applications

Establish a Start-up company for selling the Microcontroller and for providing customer support

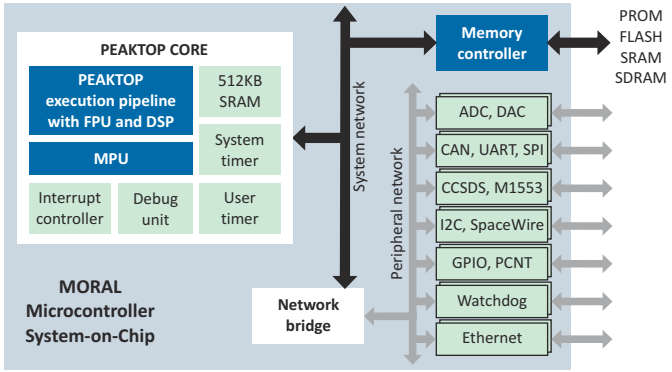

Fig. 2: MORAL - microcontroller chip architecture

NOVEL PROCESSOR ARCHITECTURE

The microcontroller is based on the completely novel PEAKTOP architecture

PEAKTOP Instruction Set Architecture (ISA)
- Simple and Flexible
- Orthogonal
- Regular
- Circular

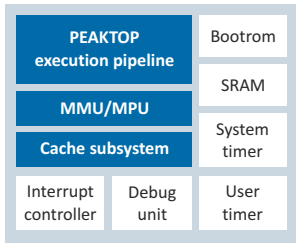

Fig. 1: PEAKTOP core

RAD-HARD COMPONENTS

Rad-hard digital libraries
Rad-hard SRAM - 512KB
Rad hard analog components: ADC, DAC

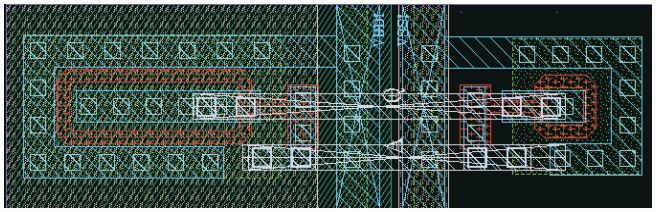

Fig. 3: Inverter gate with Edge-Less Transistors (ELT)

ON-CHIP PERIPHERALS

The MORAL chip is connected to the outside world through a memory controller providing access to FLASH, EEPROM, SRAM, SDRAM

Standard peripherals like ADC, DAC, CAN, UART, SPI, SpaceWire, GPIO, PWM, etc.

OPTIMIZING C COMPILER

AbsInt's CompCert as the first commercially-available, formally-verified, optimizing C compiler will be ported to PEAKTOP

REAL-TIME OPERATING SYSTEM

SYSGO's PikeOS real-time separation kernel with the MILS (Multiple Independent Levels of Security) approach will be ported to PEAKTOP

STRESS TESTS - TRL 7 TARGET

Stress tests will be conducted for the validation of the chip under irradiation, i.e., Total Ionizing Doze (TID) and Single Event Effects (SEE)